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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Martin Raymond Scott, et al.

Application No.: 10/652,645

Filed: August 28, 2003

For: ADAPTIVE CLOCK RECOVERY

Examiner:

Art Unit: 2661

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C.P. Marshall 2/9/2004
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Commissioner for Patents
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SUBMISSION OF CERTIFIED COPY OF PRIORITY DOCUMENTS

Sir:

Applicants hereby enclose a certified copy of two separate priority documents for the above-referenced patent application. The enclosed documents are certified copies of British Application No. GB 0220114.3, filed August 30, 2002 and British Application No. GB 0229048.4, filed December 12, 2002.

If there are any charges not covered by any check submitted, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: February 9, 2004

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The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation and Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein together with the Statement of inventorship and of right to grant of a Patent (Form 7/77), which was subsequently filed.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

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(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
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NP9 1RH

1. Your reference

JPA.P52176GB

2. Patent application number
(The Patent Office will fill in this part)

0220114.3

30AUG02 E744599-2 D01063
P01/7700 0.00-0220114.3

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Zarlink Semiconductor Limited
Cheney Manor
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Patents ADP number *(if you know it)*

8247968001

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

4. Title of the invention

Adaptive Clock Recovery

5. Name of your agent *(if you have one)*

Marks & Clerk

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

4220 Nash Court
Oxford Business Park South
Oxford OX4 2RU
United Kingdom

Patents ADP number *(if you know it)*

7271125001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	7
Claim *(s)*	2
Abstract	1
Drawing *(s)*	2 x2

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	4
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature Marks & Clerk Date 29 August 2002

Marks & Clerk

12. Name and daytime telephone number of person to contact in the United Kingdom: Julian Asquith - 01865 397900

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30 AUG 2002

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7/77

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30 AUG 2002
NEWPORT

Statement of inventorship and of right to grant of a patent

The Patent Office

Cardiff Road
Newport
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NP9 1RH

1. Your reference JPA.P52176GB

2. Patent application number *(if you know it)* 0220114.3

3. Full name of the or of each applicant
Zarlink Semiconductor Limited

4. Title of the invention
Adaptive Clock Recovery

5. State how the applicant *(s)* derived the right from the inventor *(s)* to be granted a patent
By virtue of employment

6. How many, if any, additional Patents Forms 7/77 are attached to this form?
(see note (c))

7. I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

Signature Marks & Clerk Date 29 August 2002

8. Name and daytime telephone number of person to contact in the United Kingdom Julian Asquith - 01865 397900

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Reminder

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Adaptive Clock Recovery

The invention relates to the recovery of clock signals for a TDM output from packets of TDM data which have been transmitted over a packet network.

TDM links are synchronous circuits, with a constant bit rate governed by the service clock $f_{service}$. With a packet network the connection between the ingress and egress frequency is broken, since packets are discontinuous in time. From Figure 1, the TDM service frequency $f_{service}$ at the customer premises must be exactly reproduced at the egress of the packet network (f_{regen}). The consequence of a long-term mismatch in frequency is that the queue at the egress of the packet network will either fill up or empty, depending on whether the regenerated clock is slower or faster than the original. This will cause loss of data and degradation of the service.

The relevant standards on circuit emulation services over ATM, ITU standard I.363.1 and ATM Forum standard af-vtoa-0078 refer to the concept of adaptive clock recovery in general terms.

This invention seeks to provide an adaptive method for recovering the original service clock frequency from the arrival rate of packets across the network.

According to the invention there is provided a method of recovering a clock signal, and a reference clock recovery system, as set out in the accompanying claims.

Embodiments of the invention will now be more particularly described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram showing a leased line TDM service being carried across a packet network; and

Figure 2 is a schematic diagram showing a packet count clock recovery method in accordance with an embodiment of the invention.

In Figure 1, the rate of transmission of packets from the source device is isochronous and determined by $f_{service}$. However, the rate of packet arrival at the destination device is perturbed by the intervening packet network. Packets will typically arrive in bursts separated by varying amounts of delay. The delay between successive packets and bursts will vary depending on the amount of traffic in the network. The characteristics of the network are non-deterministic, but over the long term the rate of arrival at the destination will equal the rate of departure at the source (assuming no lost or duplicate packets).

The TDM output at the destination is isochronous and determined by f_{regen}. This is provided by the Digitally Controlled Oscillator (DCO) (22) in Figure 2. The output is supplied from a Packet Delay Variation (PDV) Buffer (12). If the buffer has zero packets in it when the TDM output requires to transmit then an underrun will occur, which is undesirable. In order to minimise underrun events it is necessary to build up the PDV buffer (12) so that it contains sufficient packets to supply the TDM output for the majority of inter packet delays. However, the PDV buffer (12) cannot be made arbitrarily large because this directly increases the end to end latency which, in general, is required to be as low as possible, the maximum tolerable latency being dependent on the application. For example, voice requires lower latency than data.

Thus the optimal PDV Buffer depth depends upon network conditions and application. The clock recovery method described here allows the buffer depth to be varied independently of the clock recovery mechanism. This allows the clock recovery to stabilise prior to setting up the PDV Buffer, and allows the buffer to be changed during operation to match any underlying shift in network characteristics.

When packets arrive at the Packet Input (10) they are placed into the PDV Buffer (12) in a Queue (14). They also cause the Packet Count in Packet Counter (16) to be incremented. The Packet Count will increment by one for each packet received. The rate at which packets are received is determined by the frequency of the source TDM clock $f_{service}$. The rate at which the PDV Buffer (12) is emptied is determined by the frequency

of the destination TDM clock f_{regen}. The Packet Count is decremented by one each time that the DCO output indicates that a packet has been transmitted from the TDM output (18). Note that if the PDV Buffer (12) is empty when the TDM output (18) requests a packet, an underrun packet will be supplied to the TDM output (18). In this case the Packet Count will still be decremented. Therefore the value in the Packet Counter can be positive or negative.

Hence, given an ideal fixed delay packet network, the value of the Packet Count will increase if $f_{service}$ exceeds f_{regen} , will decrease if f_{regen} exceeds $f_{service}$, and will remain constant if the frequencies are identical.

Therefore a Clock Control Algorithm (20) can sample this value at a fixed interval (the Clock Control Interval), perform a calculation to determine a correction that can be applied in order to converge the local frequency to the source frequency, and write the new local frequency value to a DCO (22).

With a real network the value of the Packet Count fluctuates due to the burst nature of the incoming packet stream. This causes fluctuations in the recovered clock. Therefore a filter function (24) is provided on the device which provides the following benefits:

- reduces the workload of the Clock Control Algorithm (which may be implemented by an external CPU) in terms of numerical processing
- reduces the workload of the Clock Control Algorithm by allowing the Clock Control Interval to be increased
- reduces fluctuations in the recovered clock

In this embodiment the filter (24) is a first order low pass filter with the following difference equation that is simple to implement in hardware without requiring any dividers or multipliers:

$$Y_n = Y_{n-1} + (X_n - Y_{n-1})/2^P \qquad \text{(Equation 1)}$$

Where :

Y_n is the Filter Output

X_n is the Packet Count

P is a programmable parameter that determines the time constant of the filter

n is the sample number that increments each time that a packet is taken from the PDV Buffer

The Clock Control Algorithm (20) reads the Filter Output and determines the correction required to stabilise the Packet Count, and writes the required Frequency to the DCO.

A simple first order Clock Control Algorithm is given by the following difference equation:

$$F_m = \alpha F_{m-1} + \beta Y_m$$

Where:

F_m is the Frequency to be written to the DCO

α , β are constants that determine the time constant

F_{m-1} is the Current DCO Frequency

Y_m is the Filter output

m is the sample number that increments each time the Clock Control Algorithm reads the Filter Output

The time constant is selected to track long term drift in $f_{service}$ but reject short term variation due to packet delay variations.

The PDV Depth Control Algorithm (26) should make relatively infrequent adjustments to the PDV Buffer (12) which may be based on any of the following:

- Filtered Depth reading of queue depth provided by Depth Filter (28), which may be of the type described by Equation (2)
- Underrun events (indicating the Queue is too small)
- Maximum and Minimum Depth readings
- Network Delay Measurements (for example obtained by a network "ping" utility)

The Minimum & Maximum queue depth values are reset to the current Queue Depth when they are read by the PDV Buffer Depth Control Algorithm (26), and are then adjusted whenever the Packet Queue Depth is altered.

Alternative Filter algorithms may be used.

Alternative Clock Control Algorithms may be used e.g. 2^{nd} and higher order, fuzzy logic, neural networks, and self-tuning algorithms that vary parameters such as the time constant or Clock Control Interval over time.

An internal or external CPU may be used for the Clock Control & Depth Control Algorithms

Sequence numbers may be used within the packets, in which case the Packet Count increment can be made to take into account lost packets. This improves the performance of the clock recovery method in networks with a significant percentage of lost packets. In this case, when a packet arrives the following algorithm may be applied to determine the Packet Count increment. (Wraparound must also be detected and dealt with appropriately).

If $S_k > S_{k-1}$ then increment = $S_k - S_{k-1}$
Else increment = 0

Where :
S_k is the sequence number of the received packet
S_{k-1} is the sequence number of the previous received packet

Byte or Bit resolution rather than Packet resolution may be used, where the Counter value represents Bytes or Bits rather than Packets. In this case, when a packet arrives, the Counter is incremented by the number of payload bytes or bits that it contains, whereas the Counter is decremented by one whenever the DCO output indicates that a byte or bit has been transmitted by the TDM output.

The method has application in timing recovery over packet based systems or other asynchronous systems. A typical application of the method described above is in emulation of TDM (time division multiplexed) circuits across a packet network, such as Ethernet, ATM or IP. Circuit emulation may be used to support the provision of leased line services to customers using legacy TDM equipment. For example, Figure 1 shows a leased line TDM service being carried across a packet network. The advantages are that a carrier can upgrade to a packet switched network, whilst still maintaining their existing TDM business.

The clock recovery method described above provides the following advantages:

1. The method makes use of all of the incoming data packets at the destination device to converge average packet egress rate to average packet ingress rate.

2. No special timing packets or information is required.

3. No expensive Clock Generation Circuits are required (such as oven controlled crystal oscillators).

4. A Packet Counter is maintained that allows the difference between the rate at which packets are received at the packet input and the rate at which they are transmitted from the TDM output to be monitored.

5. The Packet Counter value is operated on by packet ingress and packet egress events.

6. The Packet Counter value is filtered at an appropriate interval.

7. The filtered Packet Counter value is used by a Clock Control Algorithm to adjust the egress packet rate of the device.

8. The separation of the filter from the Clock Recovery Algorithm allows the Clock Control Algorithm to operate at a much slower rate than the filter. So that, for example, a high speed filter could be implemented in Hardware and a low speed Clock Control Algorithm with an external CPU. This confers significant benefits, such as flexibility, reduction of development risk, ease of optimising the solution for a specific environment etc.

9. The method allows packets to be deleted from the PDV Buffer and dummy packets to be inserted into the PDV Buffer in order to adjust the device latency. This does not affect the counter value mentioned above.

10. The PDV Buffer Depth is filtered at an appropriate interval.

11. Minimum & Maximum PDV Buffer Depth values are maintained

12. The filtered PDV Buffer Depth, and Minimum & Maximum PDV Buffer Depth values may be used by a Buffer Depth Control Algorithm which may run at a much slower rate than the rate at which the filter is updating.

13. The PDV Buffer depth can to be varied independently of the clock recovery mechanism. This allows the clock recovery to stabilise prior to setting up the PDV Buffer, and allows the buffer to be changed during operation to match any underlying shift in network characteristics.

CLAIMS:

1. A method of recovering a clock signal for a TDM output from packets of TDM data which have been transmitted over a packet network, the method comprising:

providing a packet buffer to store incoming packets after transmission over the packet network,

maintaining a packet count which is incremented as packets arrive at the packet buffer, and decremented each time a packet leaves the packet buffer, and

sampling the packet count and controlling the clock frequency of the TDM output on the basis of the sampled packet count.

2. A method as claimed in claim 1, which further comprises:

sampling the packet count at a fixed interval,

performing a calculation to determine the source frequency of a TDM clock at the source of the packets, and

writing a new local frequency value to a digitally controlled oscillator which controls the clock frequency of said TDM output.

3. A method as claimed in claim 1 or 2, which further comprises filtering the value of the packet count before sampling the packet count.

4. A method as claimed in claim 3 wherein the filtering is carried out using a first order low pass filter.

5. A method as claimed in any preceding claim which further comprises:

making adjustments to the packet buffer, by adding or removing packets, based on at least a filtered reading of the depth of the packet buffer.

6. A reference clock recovery system, for recovering a clock signal for a TDM output from packets of TDM data which have been transmitted over a packet network, the system comprising:

a packet buffer for storing incoming packets after transmission over the packet network,

a packet counter which maintains a packet count which is incremented as packets arrive at the packet buffer, and decremented each time a packet leaves the packet buffer, and

a clock control device which samples the packet count value and controls the clock frequency of the TDM output on the basis of the sampled packet count.

7. A reference clock recovery system as claimed in claim 6, which further comprises a digitally controlled oscillator which controls the clock frequency of said TDM output,

and wherein the clock control device performs a clock control algorithm which determines the source frequency of a TDM clock at the source of the packets, and writes a new local frequency value to the digitally controlled oscillator so as to control the clock frequency of said TDM output.

8. A reference clock recovery system as claimed in claim 6 or 7, which further comprises a packet counter filter arranged to filter the value of the packet count before the value of the packet count is sampled by the clock control device.

9. A reference clock recovery system which further comprises a buffer depth control device arranged to make adjustments to the packet buffer, by adding or removing packets, based on at least a filtered reading of the depth of the packet buffer.

ABSTRACT

Adaptive Clock Recovery

A method of recovering a clock signal for a TDM output from packets of TDM data which have been transmitted over a packet network, comprises

providing a packet buffer to store incoming packets after transmission over the packet network,

maintaining a packet count which is incremented as packets arrive at the packet buffer, and decremented each time a packet leaves the packet buffer, and

sampling the packet count and controlling the clock frequency of the TDM output on the basis of the sampled packet count.

Refer to Figure 2

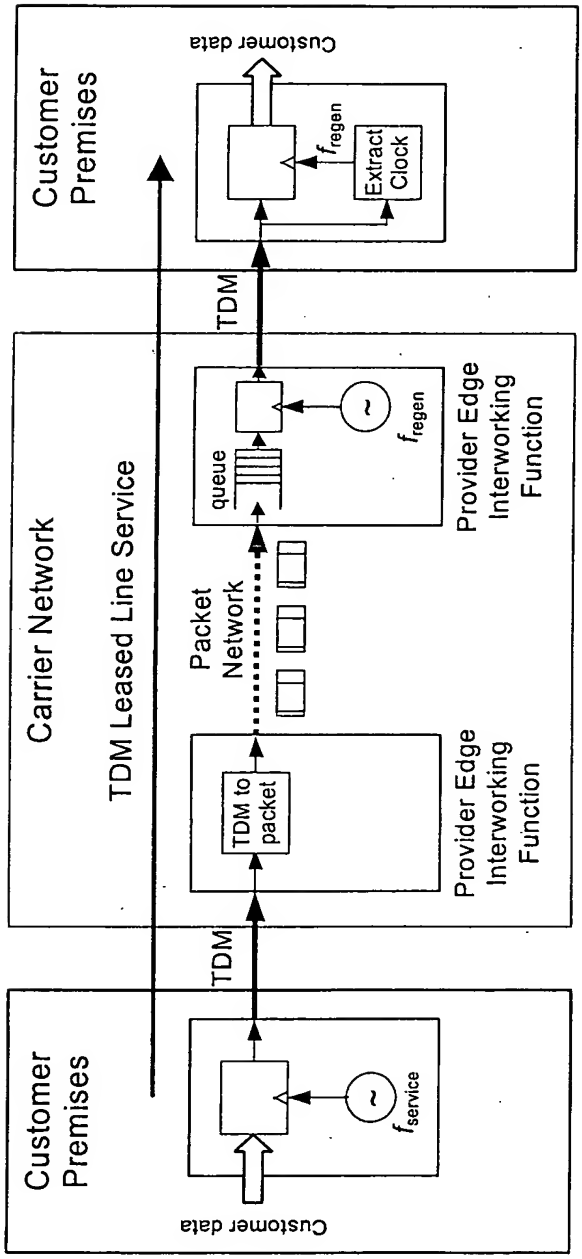
Customer Premises
Customer data
$f_{service}$
TDM
Carrier Network
TDM Leased Line Service
TDM to packet
Provider Edge Interworking Function
Packet Network
queue
f_{regen}
Provider Edge Interworking Function
TDM
Customer Premises
Customer data
f_{regen}
Extract Clock

Figure 1

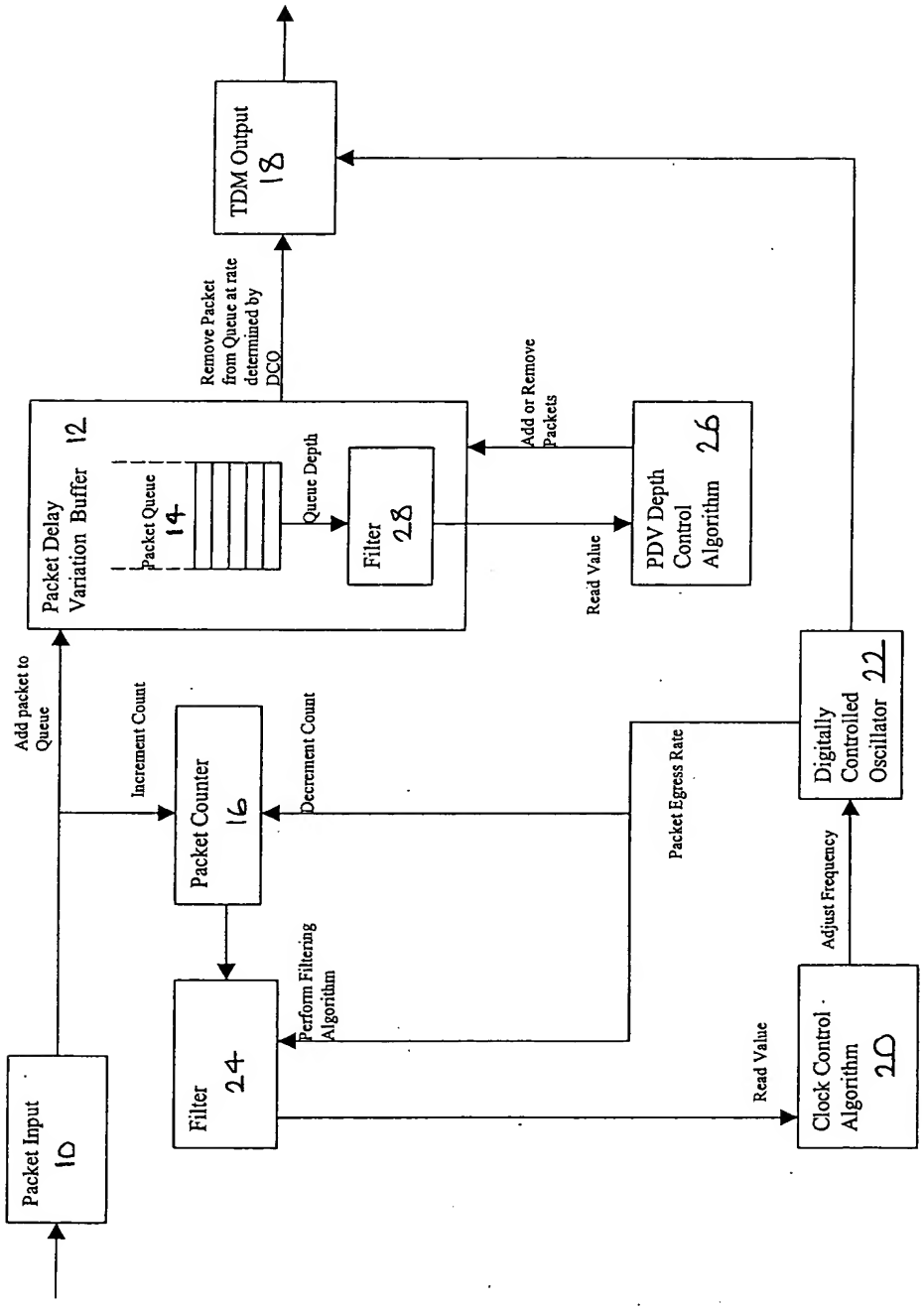
Packet Input
10
Add packet to Queue
Packet Delay Variation Buffer
12
Packet Queue
14
Queue Depth
Filter
28
Remove Packet from Queue at rate determined by DCO
TDM Output
18
Add or Remove Packets
PDV Depth Control Algorithm
26
Read Value
Increment Count
Packet Counter
16
Decrement Count
Packet Egress Rate
Digitally Controlled Oscillator
22
Perform Filtering Algorithm
Filter
24
Adjust Frequency
Read Value
Clock Control Algorithm
20

Figure 2